CLAIMS

What is claimed is:

1. A crossbar switch comprising:

a crossbar matrix that includes n input rows of cross-points and m output columns of cross-points; and

n decoders connected to said n input rows,

wherein each of said n rows includes a single serial address input between said decoder and said crosspoints.

2. The crossbar switch of claim 1 wherein each of said n rows includes a single shift input and a single data input.

3. The crossbar switch of claim 2 wherein a serial address and data enter said address input and said data input in parallel.

4. The crossbar switch of claim 3 wherein a shift sequence is transmitted on said single shift input, and wherein said data flows before said shift sequence on said shift input has completed.

5. The crossbar switch of claim 4 wherein said data is shifted through said crossbar switch using a clock.

6. The crossbar switch of claim 5 wherein said clock is generated on-chip using a clock recovery circuit.

7. The crossbar switch of claim 1 wherein said decoders convert a binary address input into a serial address.

8. The crossbar switch of claim 7 wherein said decoders include an N-bit counter including a plurality of divide-by-2 toggle flip-flops.

9. The crossbar switch of claim 1 wherein said crossbar switch is implemented using superconductor digital electronics.

10. The crossbar switch of claim 9 wherein said crossbar switch is implemented using rapid single flux quantum (RSFQ) logic.

11. The crossbar switch of claim 1 wherein one of said cross-points includes:

a nondestructive readout (NDRO) circuit having first, second and third inputs and first and second outputs, wherein said first input is connected to said serial address line, said second input is connected to a shift line, said third input is connected to a clock line;

an inverter having first and second inputs and a first output, wherein said first input of said inverter is connected to said first output of said NDRO circuit and said second input of said inverter is connected to a reset line; and

a destructive readout circuit having first and second inputs and a first output, wherein said first input is connected to said first output of said NDRO circuit and said second input is connected to a data line.

12. A crossbar switch comprising:

a crossbar matrix that includes n input rows of cross-points and m output columns of cross-points; and

n decoders connected to said n input rows,

wherein each of said n rows includes only a single serial address input and a single data input, and wherein a serial address and data enter said serial address input and said data input in parallel.

13. The crossbar switch of claim 12 wherein said data is shifted through said crossbar switch using a clock.

14. The crossbar switch of claim 13 wherein said clock is generated on-chip using a clock recovery circuit.

15. The crossbar switch of claim 12 wherein said decoders convert a binary address input into a serial address.

16. The crossbar switch of claim 12 wherein said decoder circuit includes an N-bit counter including a plurality of divide-by-2 toggle flip-flops.

17. The crossbar switch of claim 12 wherein said crossbar switch is implemented using rapid single flux quantum (RSFQ) logic.

18. The crossbar switch of claim 12 wherein one of said cross-points includes:

a nondestructive readout (NDRO) circuit having first, second and third inputs and first and second outputs, wherein said first input is connected to said serial address input, said second input is connected to a shift line, said third input is connected to a clock line;

an inverter having first and second inputs and a first output, wherein said first input of said inverter is connected to said first output of said NDRO circuit and said second input of said inverter is connected to a reset line; and

a destructive readout circuit having first and second inputs and a first output, wherein said first input is connected to said first output of said NDRO circuit and said second input is connected to said data input.

19. A crossbar switch comprising:

a crossbar matrix that includes n input rows of cross-points and m output columns of cross-points; and

n decoders connected to said n input rows,

wherein said decoders convert a binary address input into a serial address.

20. The crossbar switch of claim 19 wherein said decoder circuit includes an N-bit counter including a plurality of divide-by-2 toggle flip-flops.

21. The crossbar switch of claim 19 wherein each of said n rows includes a single serial address input and a single data input, and wherein a serial address and data enter said serial address input and said data input in parallel.

22. The crossbar switch of claim 19 wherein said crossbar switch is implemented using rapid single flux quantum (RSFQ) logic.

23. The crossbar switch of claim 19 wherein one of said cross-points includes:

a nondestructive readout (NDRO) circuit having first, second and third inputs and first and second outputs, wherein said first input is connected to said serial address input, said second input is connected to a shift line, said third input is connected to a clock line;

an inverter having first and second inputs and a first output, wherein said first input of said inverter is connected to said first output of said NDRO circuit and said second input of said inverter is connected to a reset line; and

a destructive readout circuit having first and second inputs and a first output, wherein said first input is connected to said first output of said NDRO circuit and said second input is connected to a data line.